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10/534,170	05/05/2005	Keiji Mabuchi	09792909-6249	9957

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EXAMINER	
HSU, AMY R	
ART UNIT	**PAPER NUMBER**
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/534,170	MABUCHI, KEIJI	
	Examiner	Art Unit	
	Amy Hsu	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/5/2005, 7/26/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6275259) in view of Fowler (US 6757018) further in view of Blerkom et al. (US 6870565).

Regarding Claim 1, Gowda teaches a solid-state imaging apparatus (*Fig. 1 reference number 100, image sensor)* comprising: a pixel array that includes a plurality of pixels in a two-dimensional array (*Fig. 1 reference number 102, array of pixels mxn).* Gowda teaches an AD array that includes a plurality of unit memories in a two-dimensional array corresponding to a pixel arrangement in the pixel array, each unit including an AD converter circuit (*Fig. 1 reference number 104, ADC, and Col 2 Lines 39-44 teaches that 104 can be a plurality of ADC with one corresponding to each pixel which would make it a two dimensional array corresponding to the two dimensional pixel array).* Gowda does not teach that each unit of the ADC array is and AD memory.

However, Fowler teaches an image sensor with each unit containing an ADC, also containing memory, making each unit an AD memory (*as seen in Fig. 3 and Col 4*

Lines 44-53). Fowler shows that it is well known in the art to associate an ADC and memory component in each unit of an array.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Gowda with that of Fowler to realize an ADC array where each unit performs the ADC and stores it in a memory thereby making each unit an AD memory comprising the units of an AD memory array. It would have been obvious because configurations such as that of Fowler associate the memory in the same unit as the ADC to eliminate transfer of the digitization output of each pixel to a separate memory array. Applying this concept to Gowda would eliminate the need for a separate memory array in order to save time on transferring the output to the separate memory array.

Gowda further teaches the imaging apparatus feeds electrical signals from the pixel array to the ADC (*Col 2 Lines 36-37)* and also outputs the digital values from the ADC array but does not specifically teach the circuits for pixel array scanning and memory scanning.

Blerkom teaches image device with pixel array and ADC array (*Fig .1)* with a pixel array scanning circuit (*Fig. 1 reference number 120 and 150 and Col 2 Lines 26-31 teaches these circuits select the pixels for readout)* and also teaches a AD array readout circuit (*Fig. 1 reference number 160 readout circuit).*

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Gowda in view of Fowler with the teaching of Blerkom to realize an imaging device with pixel array and corresponding ADC array

with each unit having associated memory, which reads out signals from the pixels to the AD memory and outputs digital signals from the units of AD memory. It would have been obvious because a pixel scanning circuit is necessary to physically accomplish reading out pixel signals to the ADC taught by Gowda, and memory scanning circuit would have been necessary to physically accomplish the outputting of digitized signals from the AD memory taught by Gowda in view of Fowler. Since Gowda does not teach the physical circuits but only the functions, one of ordinary skill in the art would have looked to prior art such as Blerkom to realize the position of the circuits.

Regarding Claim 2, Gowda in view of Fowler and Blerkom teach the solid-state imaging apparatus according to claim 1, Gowda further teaches the apparatus comprising an output unit that processes the digital signals output from the AD memory and outputs the processed signals to the exterior of the apparatus (*Col 2 Lines 47-49 teaches that digital values from the ADC are output for processing and Fig. 1 shows the processing circuits, and reference number 105 shows the digital output to the exterior*)

Regarding Claim 3, Gowda in view of Fowler and Blerkom teach the solid-state imaging apparatus according to claim 1, Gowda further teaches the individual pixels in the pixel array correspond to the individual unit memories in the AD memory in a one-to-one relationship (*Col 2 Lines 39-44*).

Regarding Claim 4, Gowda in view of Fowler and Blerkom teach the solid-state imaging apparatus according to claim 1, and Gowda further teaches wherein the individual pixels in the pixel array correspond to the individual unit memories in the AD memory in an N-to-one relationship wherein N>=2 (*Col 2 Lines 39-44).*

Regarding Claim 5, in view of Fowler and Blerkom teach the solid-state imaging apparatus according to claim 1. Gowda teaches the analog signals from the pixels are read to the ADC (*Col 2 Lines 36-37),* and the ADC performs AD conversion. The ADC is modified to AD memory as addressed with Claim 1. Gowda teaches the digital signals are output from the ADC (*Col 2 Lines 47-49).* Blerkom teaches the physical circuits to perform these functions as addressed with Claim 1.

Regarding Claim 8, Gowda in view of Fowler teach an imaging apparatus with an AD memory array, where each unit of the array performs AD conversion and storage of the digital result. Fowler is silent on the specific hardware of the memory that is taught, but it would have been obvious to one of ordinary skill in the art at the time of the invention to use DRAM for the memory because of its structural simplicity and ability to reach high density.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6275259) in view of Fowler (US 6757018) and Blerkom et al. (US 6870565), further in view of Pain et al. (US 7268814).

Regarding Claim 6, Gowda teaches an ADC which is an array with one ADC per pixel, which one skilled in the art realizes is used for the advantage of simultaneously performing AD conversion of each pixel signal. Pain teaches in Col 4 Lines 29-36 that an ADC in an imaging array can be an ADC array the same size as the pixel array so that all the output signals from the pixels can be digitized in parallel. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Gowda which teaches an ADC array with one ADC per pixel, to simultaneously perform analog to digital conversion to save on processing time.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6275259) in view of Fowler (US 6757018) and Blerkom et al. (US 6870565), further in view of Bell et al. (US 7106372) and Pain et al. (US 7268814).

Regarding Claim 7, Gowda teaches the electrical signals from the pixels are fed to the ADC (*Col 2 Lines 36-37),* but does not teach specifically it is read row by row. Bell teaches in Col 4 Lines 54-58 that read out of a pixel array to an ADC is read out on a per row basis. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Gowda with that of Bell to read out the pixels row by row to the ADC in the case of having one ADC per row. Gowda teaches the ADC is not limited to any configuration and can be one ADC per row; in this case it

would have been obvious to read the pixels out by rows to each row's corresponding ADC. The AD conversion is performed in parallel as described with Claim 6.

5. Claim 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6275259) and Fowler (US 6757018) in view of Pain et al. (US 7268814).

Regarding Claim 9, Gowda in view of Fowler teach a solid-state imaging apparatus comprising: a pixel array that includes a plurality of pixels in a two-dimensional array; and an AD memory that stores signals read from the pixel array and carries out AD conversion on these signals, the AD memory including a plurality of unit memories at least in a two-dimensional array (*as addressed with Claim 1)* and the plurality of unit memories simultaneously carrying out AD conversion on signals from at least two rows of pixels (*as addressed with Claim 6).*

Regarding Claim 10, Pain teaches an ADC array can be one ADC per column and also teaches multiple ADC should be used in parallel. If the ADCs are arranged per column, each would be carrying out conversion on a combination of signals from the pixel array, from each column. Each ADC would be converting pixels from each column in parallel. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Gowda in view of Fowler, a pixel array with corresponding AD memory array, with that of Pain to realize the parallel

receive signals from a combination of pixels and perform digitization in parallel, or simultaneously.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6275259) and Fowler (US 6757018) in view of Pain et al. (US 7268814), further in view of Blerkom et al. (US 6870565).

Regarding Claim 11, Gowda in view of Fowler teach an imaging apparatus with a pixel array and corresponding AD memory array. However they do not teach the AD memory carries out noise removal. Blerkom teaches that integrating ADC array on the same substrate as the pixel array is a way of removing noise (*Col 2 Lines 10-17).* It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teaching of Gowda in view of Fowler and to apply the teaching of Blerkom to perform noise removal on the same place the AD conversion is performed, which is the AD memory array. It would be obvious to carry out noise removal and AD conversion on the signals from the pixel array because combining the ADC and the memory for each unit eliminates noise which would be created when transferring the output of the ADC to a separate memory array.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Mansoorian et al. (US 6400824) teaches an imaging device photosensing array with at least one ADC.

Krymski (US 6885331) teaches a storage capacitor array and ADC circuit.

Shaw et al. (US 6606122) teaches a pixel array with row drivers and ADC.

Fossum (US 6847398) teaches an APS array with corresponding ADC array.

Toyoda (US 7136097) teaches an ADC array for each row of photodetectors in an array.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amy Hsu whose telephone number is 571-270-3012. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amy Hsu
Examiner
Art Unit 2622

ARH 11/21/07

LIN YE
SUPERVISORY PATENT EXAMINER